In the Claims:

Please amend claims 1, 5-6, 14, 17-21, 25 and 27, as indicated below.

1. (Currently amended) A microprocessor, comprising:

a dispatch unit configured to dispatch load and store operations; and

a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit, wherein the load store unit includes a STLF (Store-to-Load Forwarding) buffer, wherein the STLF buffer includes a plurality of entries;

wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to use the index to select one of the plurality of entries, and to forward data included in the one of the plurality of entries as a result of the load operation.

2. (Original) The microprocessor of claim 1, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation

3. (Original) The microprocessor of claim 1, wherein the one of the plurality of entries in the STLF buffer is configured to store an address, data, and a data size associated with a store operation.

4. (Original) The microprocessor of claim 1, wherein each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation.

5. (Currently amended) The microprocessor of claim 1, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation.

6. (Currently amended) The microprocessor of claim 5, wherein the load store unit is configured to generate the additional index dependent on both the at least ~~the~~ a portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein the load store unit is configured to generate the index dependent on both the at least ~~the~~ a portion of the address of the load operation and a number of bytes of data operated on by the load operation.

7. (Original) The microprocessor of claim 6, wherein the additional index is generated by right-shifting a lower portion of the address targeted by the store operation by an amount equal to a logarithm in base two of the number of bytes of data operated on by the store operation.

8. (Original) The microprocessor of claim 5, wherein the additional index comprises a portion of the address targeted by the store operation.

9. (Original) The microprocessor of claim 1, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer.

10. (Original) The microprocessor of claim 9, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation.

11. (Original) The microprocessor of claim 9, wherein the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer.

12. (Original) The microprocessor of claim 9, wherein the STLF checker is configured to replay one or more additional operations that are dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer.

13. (Original) The microprocessor of claim 9, wherein the load store unit is configured to identify the result of the load operation as a speculative value in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation; wherein if the STLF checker verifies that the STLF buffer operated correctly for the load operation, the load store unit is configured to indicate that the result of the load operation is not speculative.

14. (Currently amended) A computer system, comprising:

a system memory; and

a microprocessor coupled to the system memory, comprising:

a dispatch unit configured to dispatch load and store operations; and

a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit, wherein the load store unit includes a STLF (Store-to-Load Forwarding) buffer, wherein the STLF buffer includes a plurality of entries;

wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to use the index to select one of the plurality of entries, and to forward data included in the one of the plurality of entries as a result of the load operation.

15. (Original) The computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the

result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation

16. (Original) The computer system of claim 14, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation.

17. (Currently amended) The ~~microprocessor~~ computer system of claim 16, wherein the load store unit is configured to generate the additional index dependent on both the at least ~~the~~ a portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein the load store unit is configured to generate the index dependent on both the at least ~~the~~ a portion of the address of the load operation and a number of bytes of data operated on by the load operation.

18. (Currently amended) The ~~microprocessor~~ computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer.

19. (Currently amended) The ~~microprocessor~~ computer system of claim 18, wherein the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer.

20. (Currently amended) A method, comprising:

receiving an address of a load operation;

generating an index corresponding to the address;

using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer; and

forwarding data included in the entry as a result of the load operation.

21. (Currently amended) The method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation.

22. (Original) The method of claim 20, further comprising the entry storing an address, data, and a data size associated with a store operation.

23. (Original) The method of claim 20, wherein each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation.

24. (Original) The method of claim 20, further comprising selecting which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation.

25. (Currently amended) The method of claim 24, wherein said generating the additional index is dependent on both the at least ~~the~~ a portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein said generating the index is dependent on both the at least a portion of the address of the load operation and a number of bytes of data operated on by the load operation.

26. (Original) The method of claim 25, wherein said generating the additional index comprises right-shifting a lower portion of the address targeted by the store operation by an amount equal to a logarithm in base two of the number of bytes of data operated on by the store operation.

27. (Currently amended) The method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation.

28. (Original) The method of claim 20, further comprising verifying operation of the STLF buffer by performing an associative address comparison to identify all issued store operations targeting a same address as the load operation and implementing a find-first algorithm to select a youngest issued store operation that is older than the load operation.

29. (Original) The method of claim 28, further comprising replaying the load operation if said verifying identifies incorrect operation of the STLF buffer.

30. (Original) The method of claim 28, further comprising replaying one or more additional operations that are dependent on the load operation if said verifying detects incorrect operation of the STLF buffer.

31. (Original) The method of claim 28, further comprising:

identifying the result of the load operation as a speculative value in response to forwarding the data in the entry included in the STLF buffer as the result of the load operation; and

if said verifying verifies that the STLF buffer operated correctly for the load operation, indicating that the result of the load operation is not speculative.